ECE 2030, Intro. To Computer Eng., QUIZ 2

Quiz No. 1: Feb. 23, 2004
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RULES.

i. This quiz is closed book.

ii. Calculators may not be used.

iii. Answer all questions and show all work to receive full credit.

iv. All questions have the same weight. (20 Points). All sub-questions within a question are weighted equally.

v. Please do not ask the proctors any questions during the exam about exam questions. Part of the test is understanding the question as written, without supplemental information. If you feel additional data is needed to solve the problem, make (and state) an assumption and then work the problem.

Question 1 – Mixed-Logic and DeMorgan’s Square
Use the mixed logic technique to design a logic circuit for \(((A+B') (A'+B)) + C'\) using only inverters and NAND gates. The inputs available are A, B, and C.

Initial Diagram:

![Initial Diagram](image1)

Intermediate Form:

![Intermediate Form](image2)

Final form (standard gate symbols):

![Final form](image3)
2. Sequential Logic

The following is an negative edge triggered latch. Shown are the Input "D" and Clock "C" signals as functions of time "t". Draw in the output Q(t) signal.

```
0 1
```

Data
0 1

Clock
0 1

Q
0 1

Question 3. Combinatorial Building Blocks

Draw a circuit that uses a 4-bit Encoder to convert a 4-pole switch's output (shown) to drive a 4:1 Multiplexer that selects 1 of 4 data lines to an output line. Also output the 2-bit number N indicating which line is selected. Label the inputs and outputs on the building blocks (Data - "D", Address "Si", Outputs "Qi") and complete the connections.

```

Switch, 1 of 4 = 1

Data 0
Data 1
Data 2
Data 3

Encoder
S0
S1
S2
S3

Mux
D0
D1
D2
D3

N1
N0

Q

Q0

Q1

Address

Data N
```

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**Question 4 – State Machine** Draw a state diagram for a Mealy machine with 3 states that outputs a "1" on every third "1" received as input, no matter how many "0"s are intermingled. For example:

**Input:** 010110100101110110110
**Output:** 00001000000100010010

![State Diagram](image)

Fill in the truth table for the logic that is needed. P1,P0 is the present state, Number the states such that 2*P1 + P0 is the number of 1's seen in the present sequence of 3. N1,N0 the next state.

<table>
<thead>
<tr>
<th>P0</th>
<th>P1</th>
<th>Input</th>
<th>N0</th>
<th>N1</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

**Question 5 – Binary and Hex Numbers.** Write the missing unsigned integer numbers in binary, hex, and normal decimal representations. Do your calculations on the back of page 2.

<table>
<thead>
<tr>
<th>Decimal</th>
<th>Hex</th>
<th>Binary</th>
</tr>
</thead>
<tbody>
<tr>
<td>189</td>
<td>BD</td>
<td>1011 1101</td>
</tr>
<tr>
<td>74</td>
<td>4A</td>
<td>0100 1010</td>
</tr>
<tr>
<td>163</td>
<td>A3</td>
<td>1010 0011</td>
</tr>
<tr>
<td>131</td>
<td>0x83</td>
<td>1000 0011</td>
</tr>
<tr>
<td>165</td>
<td>A5</td>
<td>1010 0101</td>
</tr>
<tr>
<td>83</td>
<td>0x53</td>
<td>0101 0011</td>
</tr>
</tbody>
</table>

Convert this 4-byte 2's compliment binary number to a sign and decimal magnitude:

\[1111 1111 1111 1111 1111 1111 1101 1010 = -0000 0000 0000 0000 0000 0000 0000 0000 0010 0110 = -(2\times16) + 6 = \mathbf{-38}\]