MIPS modules for Lab-4, Data Forwarding

**IFE**
- Change clock phase for “Data Memory” and Reg-Set “Write_Data” (write on negative edge).
  - Inputs to Data Forward Control

**ID**
- after<3>

**EX**
- after<2>

**MEM**
- after<1>

**WB**
- add $14, …

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Move RegWrite to IDE

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IDE

**CTL**

**ALUSrc**

**RegWrite**

**Write Data**

**Address**

**Instruction memory**

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**MEM**

**Write Data**

**Address**

**Data Memory**

---

**WriteReg**

**Data Forward Control**

---

**Add**

---

**RegDst**

**ALUOp**

**Branch**

---

**WriteReg**

**ALU result**

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**RegWrite**

**RegWrite**

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**IF**

- after<4>