Lecture 3
CPU - Data Path for Branches
Reading - Pat. & Hen. Chap. 5, Sec. 1-6

"A" means 5-bit address of register

Example: Counter
S3 S2 S1 S0
0 0 0 0
0 0 0 1
0 0 1 0
0 0 1 1
0 1 0 0

Combinatorial Logic
Branching Jumps, or use offset from array base address

Using a 16-bit Offset to form a 32-bit Address

Calculate new PC from a 16-bit Word Offset
Fig. 5.10

Datapath for Load/Store Word, ALU op.s, and Branches

Fig. 5.11

Multiplexors for Branch and Jump Operations

Fig. 5.15

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<th>ALU0</th>
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<th>ALU2</th>
<th>ALU3</th>
<th>ALU4</th>
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</table>
Single-Cycle CPU - requires 2 ALUs and separate memories for instructions and data.

A Multi-Cycle CPU (Datapath) needs additional registers to hold data between cycles. Notice the common memory for data and instructions (code).
Finite State Machine Implementation

Fig. 5.37

Combinatorial Control Logic

Datapath Control Outputs (for present state)

Inputs

Next State

State Register

Inputs from Instruction Register Opcode Field

Two new registers are added to handle Exceptions and Interrupts the EPC (Exception Program Counter) and the Cause Reg.s. (see Patterson & Hennessy Appendix A.7 on CDROM)

Fig. 5.39