Name _____ GT#_____

ECE 2030b, Intro. To Computer Eng., QUIZ 2

Quiz No. 2: Oct. 23, 2002
Prof. John A. Copeland
School of Electrical and Computer Engineering

RULES.

i This quiz is closed book.

ii. No calculators may be used.

iii Answer all questions and show all work to receive full credit.

iv All questions have the same weight. (20 Points). All sub-questions within a question are weighted equally.

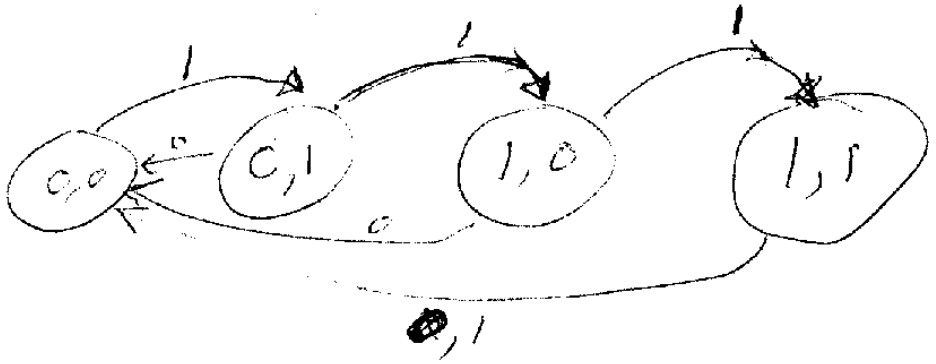
v Please do not ask the proctors any questions during the exam about exam questions. Part of the test is understanding the question as written, without supplemental information. If you feel additional data is needed to solve the problem, make (and state) an assumption and then work the problem.

Question 1. State Diagram

Draw the State Diagram for a two-bit counter (output is C1,C0) that counts the number of 1's in a row (from input X). X=0, or a fourth 1 in a row, resets the counter output, C1, C2, to 0,0. Use a Moore Machine design. Choose the state addresses so that the two-bit state address is the same as the count. Show any unused states.

Example Operation:

```
   X:  0 0 1 1 1 1 1 1 0 0 1 1 0 0 0
   C1: 0 0 0 1 1 0 0 1 0 0 0 1 0 0 0
   C0: 0 0 1 0 1 0 1 0 0 0 1 0 0 0 0
Count: 0 0 1 2 3 0 1 2 0 0 1 2 0 0 0
```



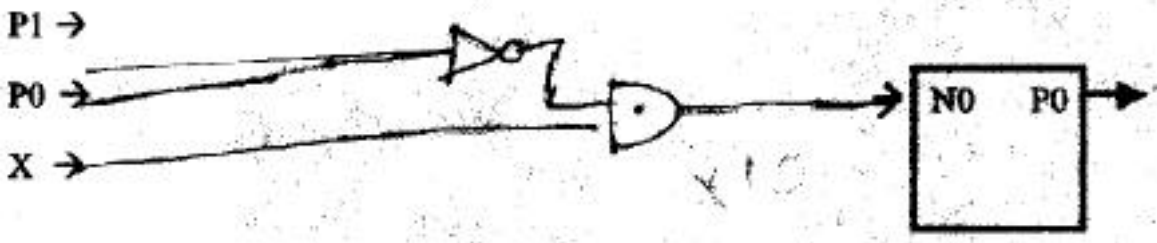
Question 2 – Truth Table for Above (Based on Example Operation)

Draw a Truth Table based on the "Example Operation." The inputs are the present values of the state C1,C0 (e.g., P1,P0) and X. The results are the next values of the state (e.g. N1,N0). The only output is P1,P0 since we chose the state name bits to correspond to the count value.

P1	P0	X	N1	N0
0	0	0	0	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	1
1	1	0	0	0
1	1	1	0	0

Question 3 – Design the circuit.

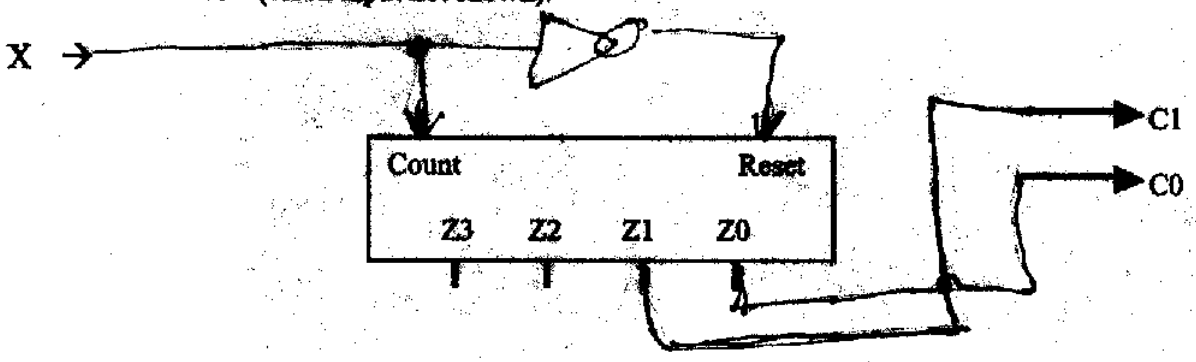
Two its are needed, to calculate N1 and N0 from P1, P0 and X.
Use t orksheet.





Question 4- Counter

Design a circuit with the same functionality as above by putting "glue" logic around a Synchronous Counter circuit shown below (clock input not shown).



Question 5 - Registers

Complete the timing diagram for the Register shown below showing the values at internal point A and output B.. Each "transparent latch" is "transparent" when the clock signal, "phi 1" or "phi 2" is high. Assume the values at A and B are "0" at the start.

