0 Name _____ GT#_____

ECE 2030, Intro. To Computer Eng., QUIZ 2 Seat No._____

Quiz No. 1: Feb. 23, 2004
Prof. John A. Copeland
School of Electrical and Computer Engineering

RULES.

i This quiz is closed book.

ii. Calculators may not be used.

iii Answer all questions and show all work to receive full credit.

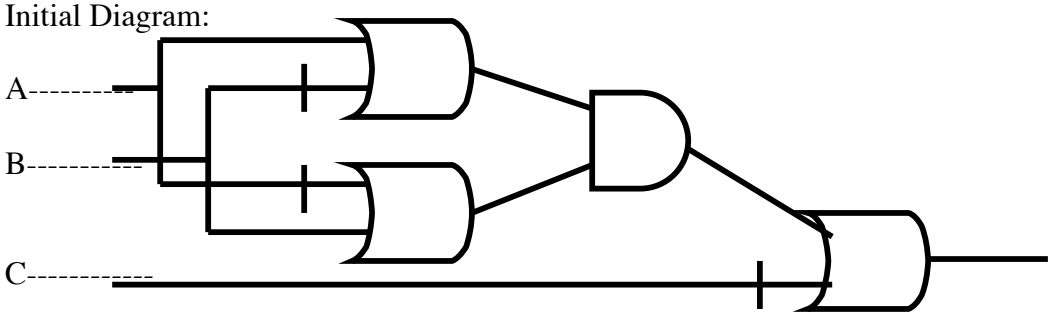
iv All questions have the same weight. (20 Points). All sub-questions within a question are weighted equally.

v Please do not ask the proctors any questions during the exam about exam questions. Part of the test is understanding the question as written, without supplemental information. If you feel additional data is needed to solve the problem, make (and state) an assumption and then work the problem.

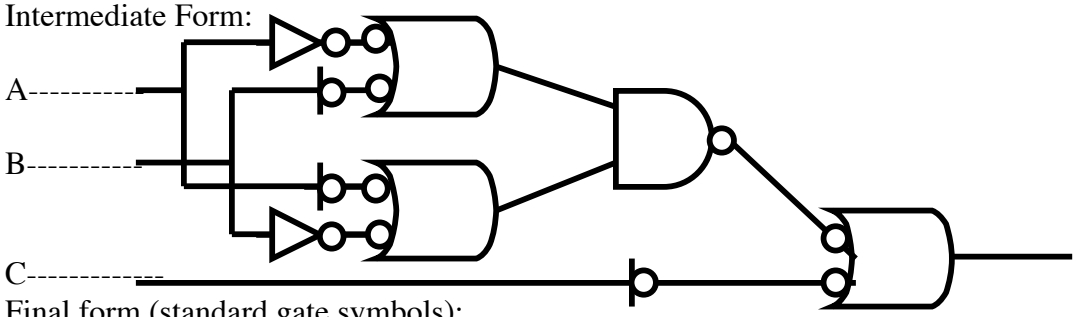
Question 1 –Mixed-Logic and DeMorgan's Square

Use the mixed logic technique to design a logic circuit for ((A+B') (A'+B)) + C' using only inverters and NAND gates. The inputs available are A, B, and C.

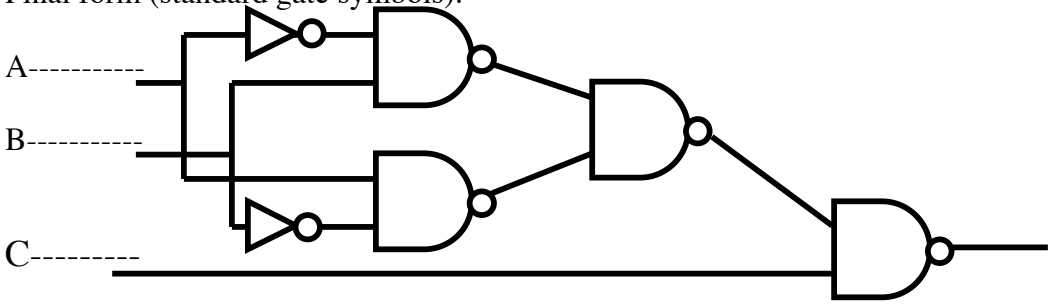
Initial Diagram:



Intermediate Form:



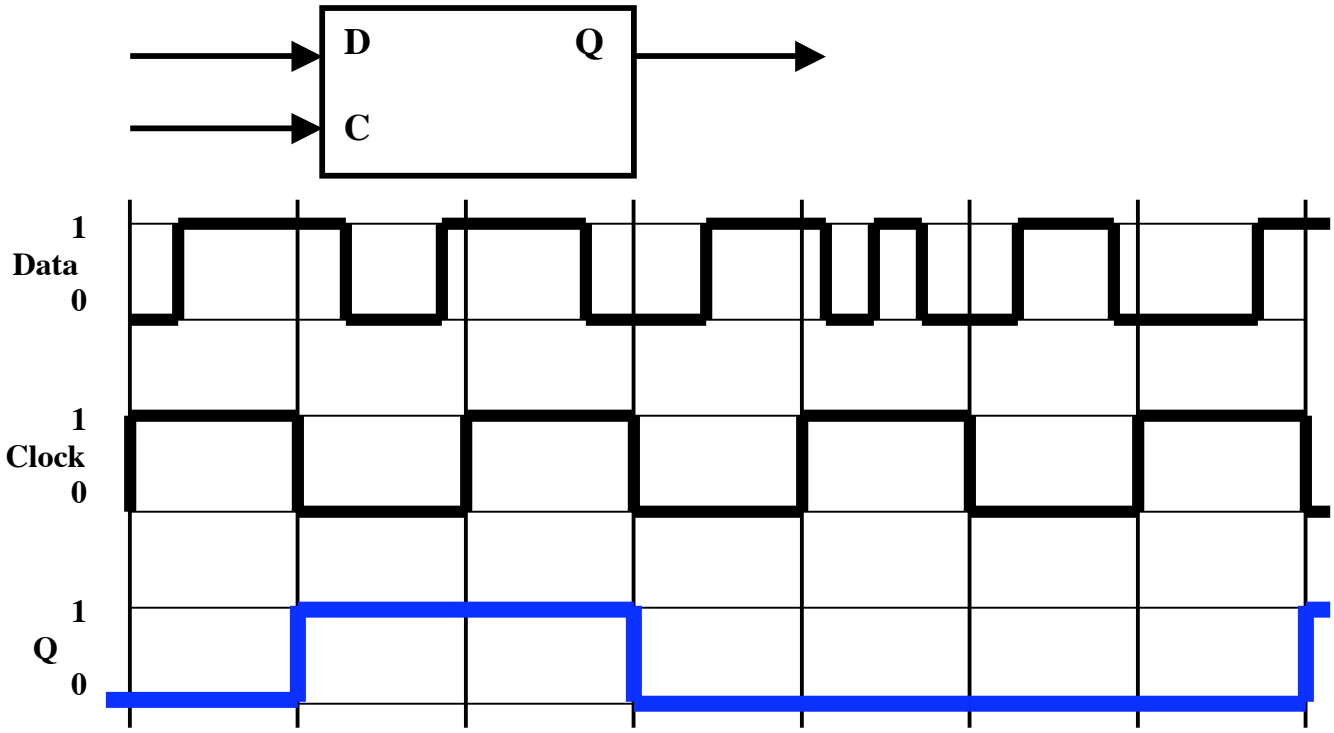
Final form (standard gate symbols):



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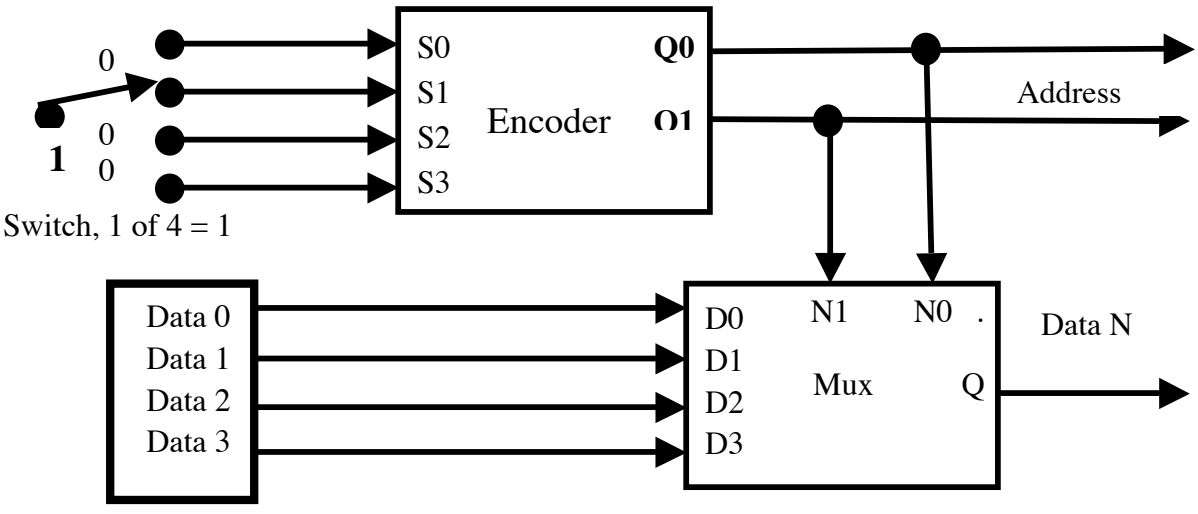
2. Sequential Logic

The following is an negative edge triggered latch Shown are the Input "D" and Clock "C" signals as functions of time "t". Draw in the output Q(t) signal.



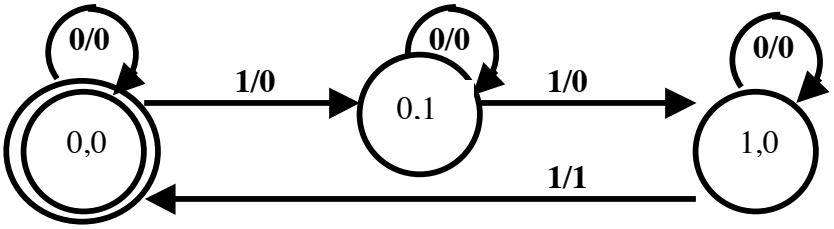
Question 3. Combinatorial Building Blocks

Draw a circuit that uses a 4-bit Encoder to convert a 4-pole switch's output (shown) to drive a 4:1 Multiplexer that selects 1 of 4 data lines to an output line. Also output the 2-bit number N indicating which line is selected. Label the inputs and outputs on the building blocks (Data - "D", Address "Si", Outputs "Qi") and complete the connections.



Question 4 – State Machine Draw a state diagram for a Mealy machine with 3 states that outputs a "1" on every third "1" received as input, no matter how many "0"s are intermingled. For example:

```
Input:  01011010010111011011 0
Output: 00001000000100010001 0
```



Fill in the truth table for the logic that is needed. P1,P0 is the present state, Number the states such that 2*P1 + P0 is the number of 1's seen in the present sequence of 3. N1,N0 the next state.

P0	P1	Input	N0	N1	Output
0	0	0	**0**	**0**	**0**
0	0	1	**0**	**1**	**0**
0	1	0	**0**	**1**	**0**
0	1	1	**1**	**0**	**0**
1	0	0	**1**	**0**	**0**
1	0	1	**0**	**0**	**1**

Question 5 – Binary and Hex Numbers. Write the missing unsigned integer numbers in binary, hex, and normal decimal representations. Do your calculations on the back of page 2.

Decimal	Hex	Binary
189	**BD**	**1011 1101**
74	4A	**0100 1010**
163	**A3**	1010 0011
131	**0x83**	**1000 0011**
165	A5	**1010 0101**
83	**0x53**	0101 0011

Convert this 4-byte 2's compliment binary number to a sign and decimal magnitude:

1111 1111 1111 1111 1111 1111 1101 1010 =
= - 0000 0000 0000 0000 0000 0000 0010 0110 = - (2x16) + 6 = **-38**