0 Name _____ GT#_____

ECE 2030, Intro. To Computer Eng., QUIZ 3 Seat No._____

Quiz No. 3: Apr. 2, 2004
Prof. John A. Copeland
School of Electrical and Computer Engineering

RULES.

i This quiz is closed book.

ii. Calculators may not be used.

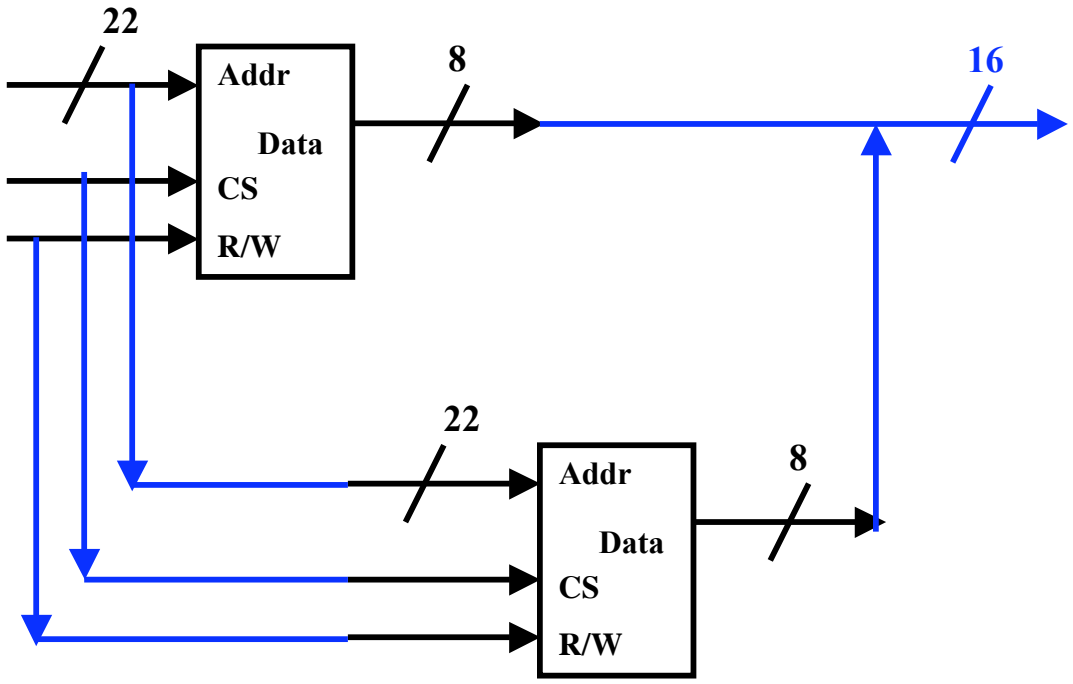
iii Answer all questions and show all work to receive full credit.

iv All questions have the same weight. (20 Points). All sub-questions within a question are weighted equally.

v Please do not ask the proctors any questions during the exam about exam questions. Part of the test is understanding the question as written, without supplemental information. If you feel additional data is needed to solve the problem, make (and state) an assumption and then work the problem.

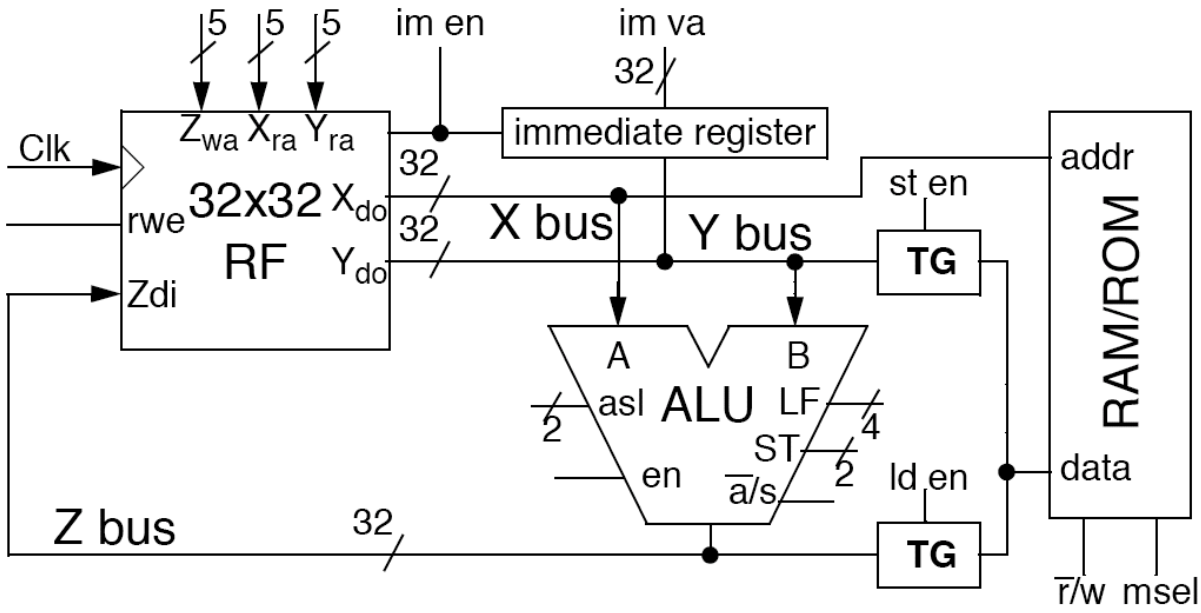
Question 1 – Memory Chips

Show how to connect these 4M x 8 chips to make a 4M by 16 memory.



2. Datapath

In the table below, show the datapath control signals needed to read a 32-bit word from RAM address $3 (already in register 3), add it and $5, then write the sum to the same RAM address.



$1 = M[$3]
$1 = $1 + $5
M[$3] = $1

asl 0 = arithmetic, 1, = shift, 2 = logic, 3 = invalid
a'/s 0 = add, 1 = subtract
en 0 = off, 1 = on

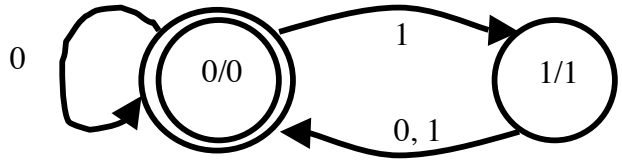
Mem r'/w	X (5 bit)	Y (5 bit)	Z (5 bit)	rwe	asl (2 bit)	a'/s	en	ld en	st en	im en	im va (32 bit)
0	3	X	1	1	X	X	0	1	0	0	X
0	1	5	1	1	0	0	1	0	0	0	X
1	3	1	X	0	X	X	0	0	1	0	X

3. Shift Registers - Starting with the bits in the top row, show the result of the six different shifts indicated. Do not start with the previous answer.

Starting Bits	1	1	1	0	1	1	0	0
Logical Right 3	0	0	0	1	1	1	0	1
Arithmetic Right 3	1	1	1	1	1	1	0	1
Rotate Right 3	1	0	0	1	1	1	0	1
Logical Left 3	0	1	1	0	0	0	0	0
Arithmetic Left 3	0	1	1	0	0	0	0	0
Rotate Left 3	0	1	1	0	0	1	1	1

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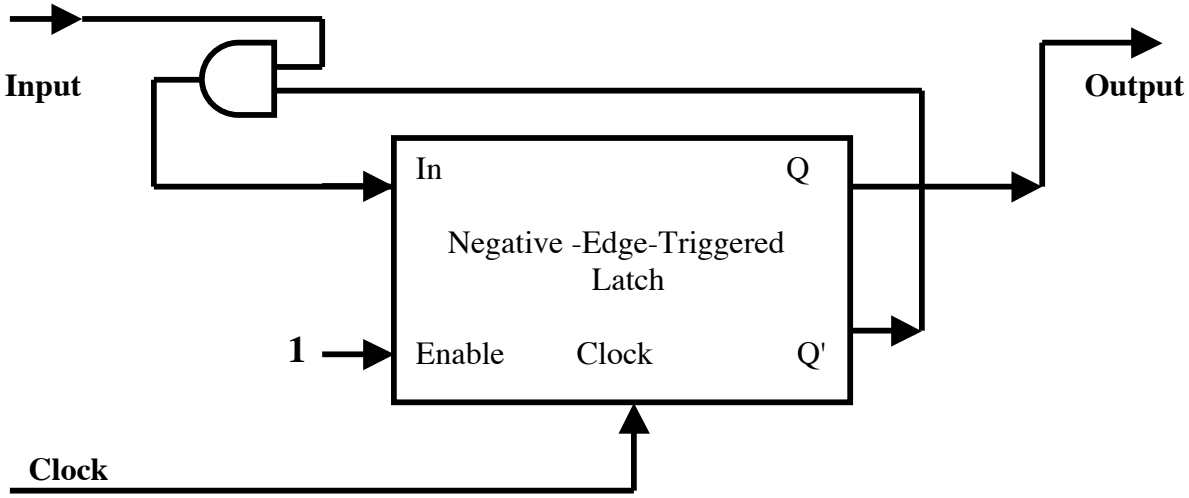
Question 4 – State Machine This is the State Diagram for a Moore machine with 2 states.



Fill in the truth table for the logic that is needed. P is the present state, Number the states such that P is the number of 1's seen in the present sequence of 2. N the next state.

P0	Input	N0	Output
0	0	**0**	**0**
0	1	**1**	**0**
1	0	**0**	**1**
1	1	**0**	**1**

Design the logic to implement the above state machine using AND, OR, and NOT gates and the negative-edge triggered latch below.



Question 5 - Complete the table below. A "2M x 16" memory has 2M words of 16 bits.

Memory	Total Bits	# of addresses	# of address lines	# of data lines
4M x 32	**128M**	**4M**	**22**	**32**
1Mx8	**8M**	**1M**	**20**	**8**
64Kx32	**2M**	**64K**	**16**	**32**
1Kx8	**8K**	**1K**	**10**	**8**
64Kx16	**1M**	**64K**	**16**	**16**