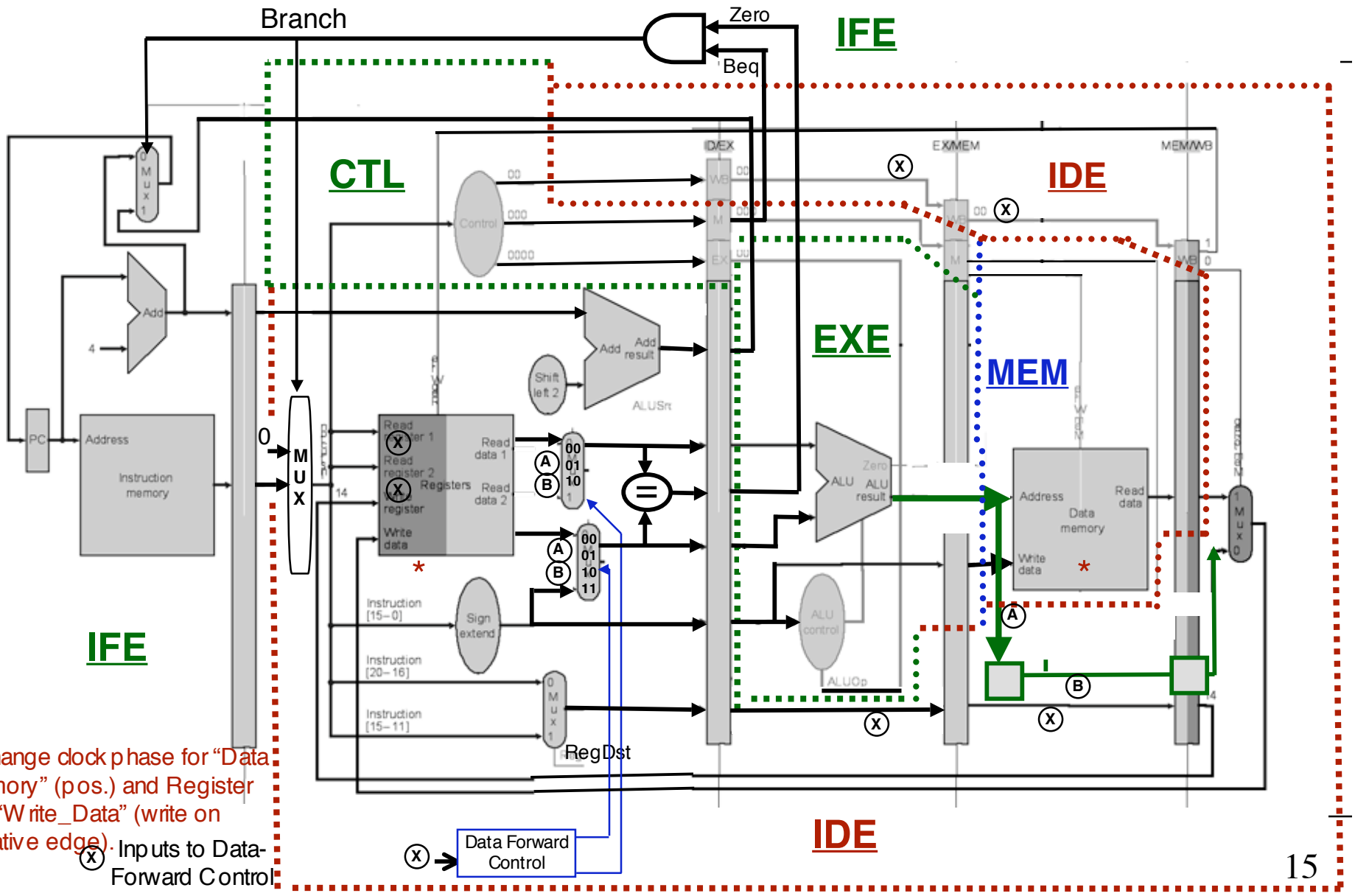
MIPS modules for Lab-5, Branch Handling



* Change clock phase for "Data Memory" (pos.) and Register Set "Write_Data" (write on negative edge).

(X) Inputs to Data-Forward Control